

FIG. 1

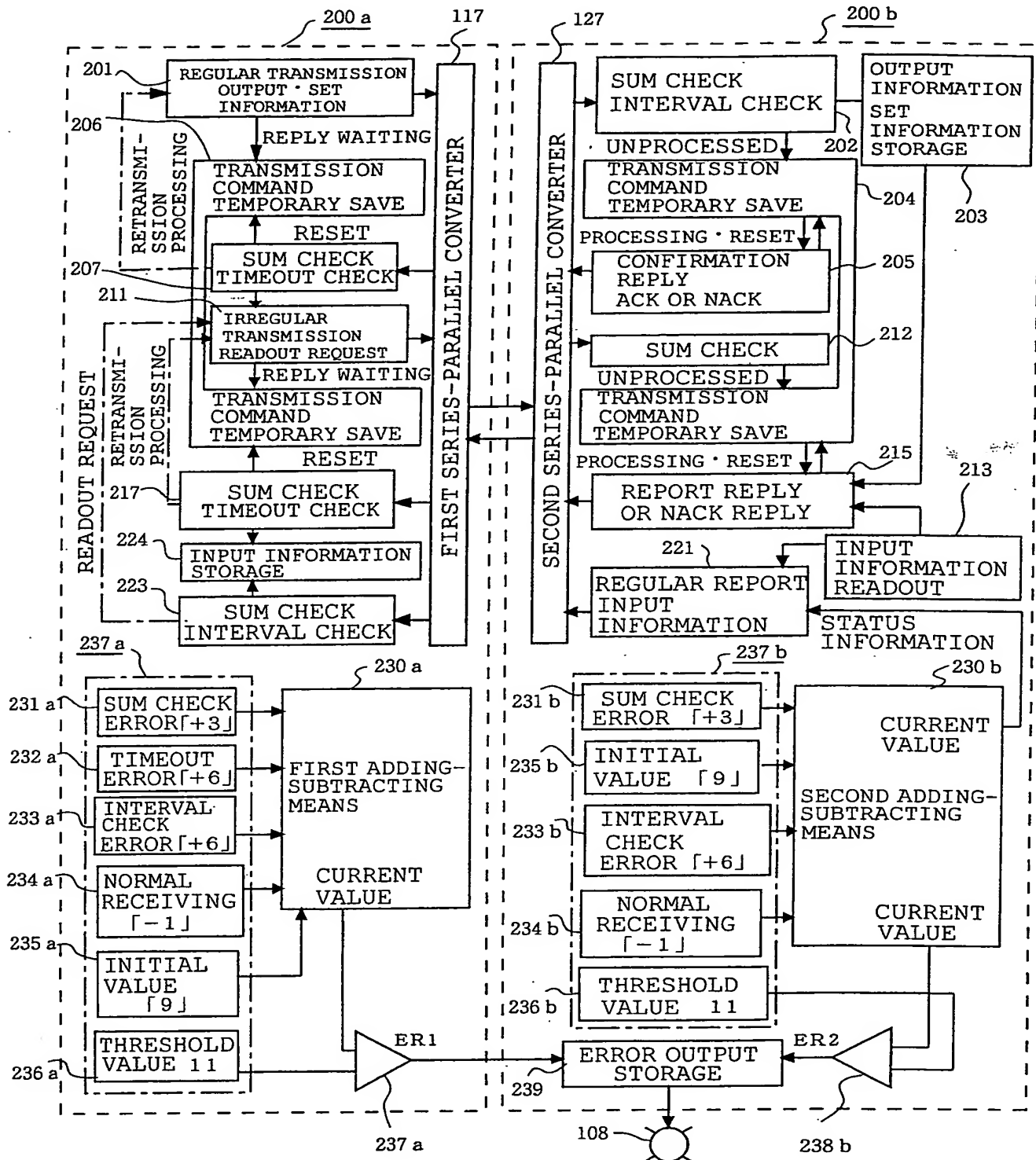


FIG. 2

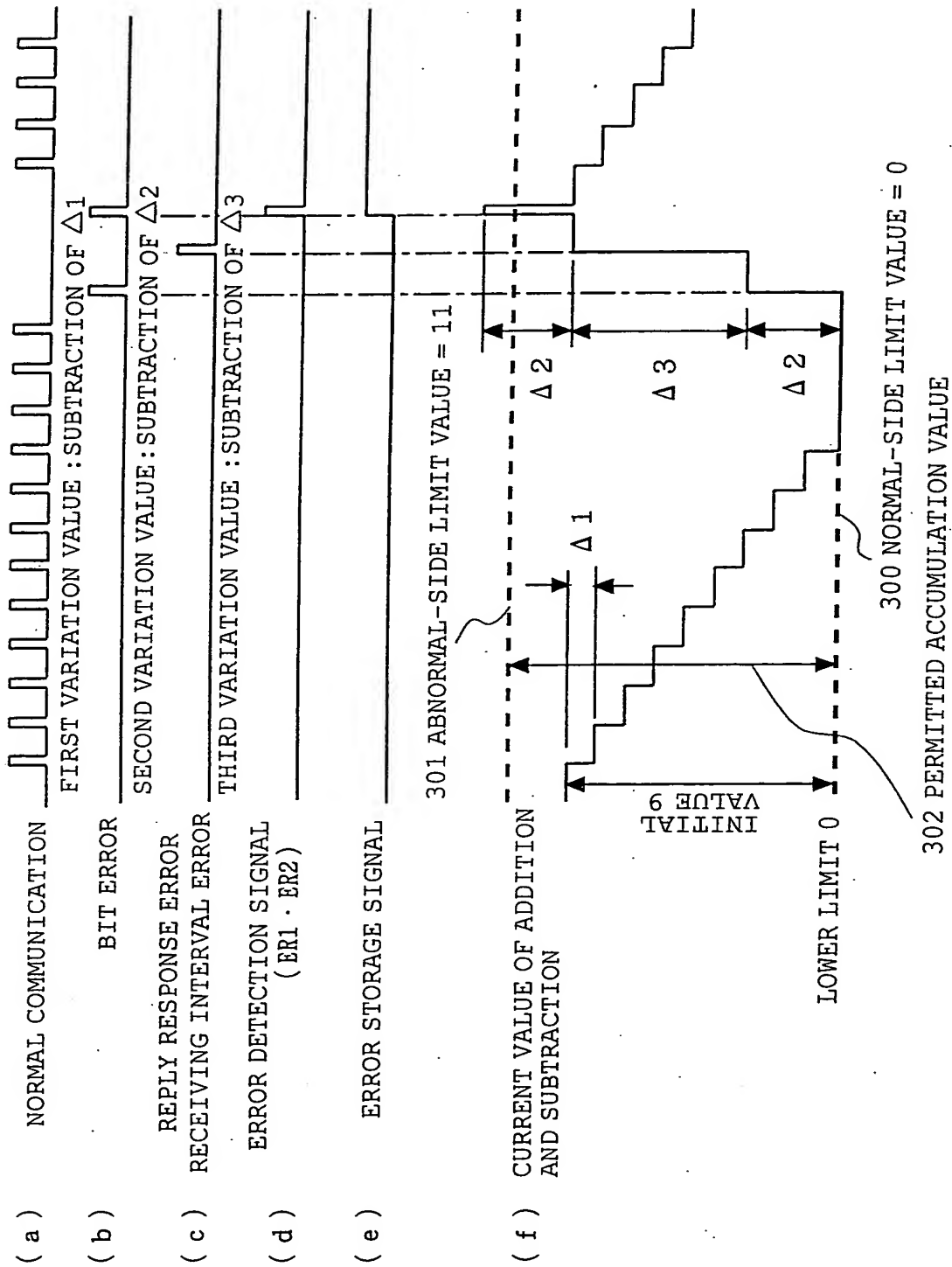


FIG. 3

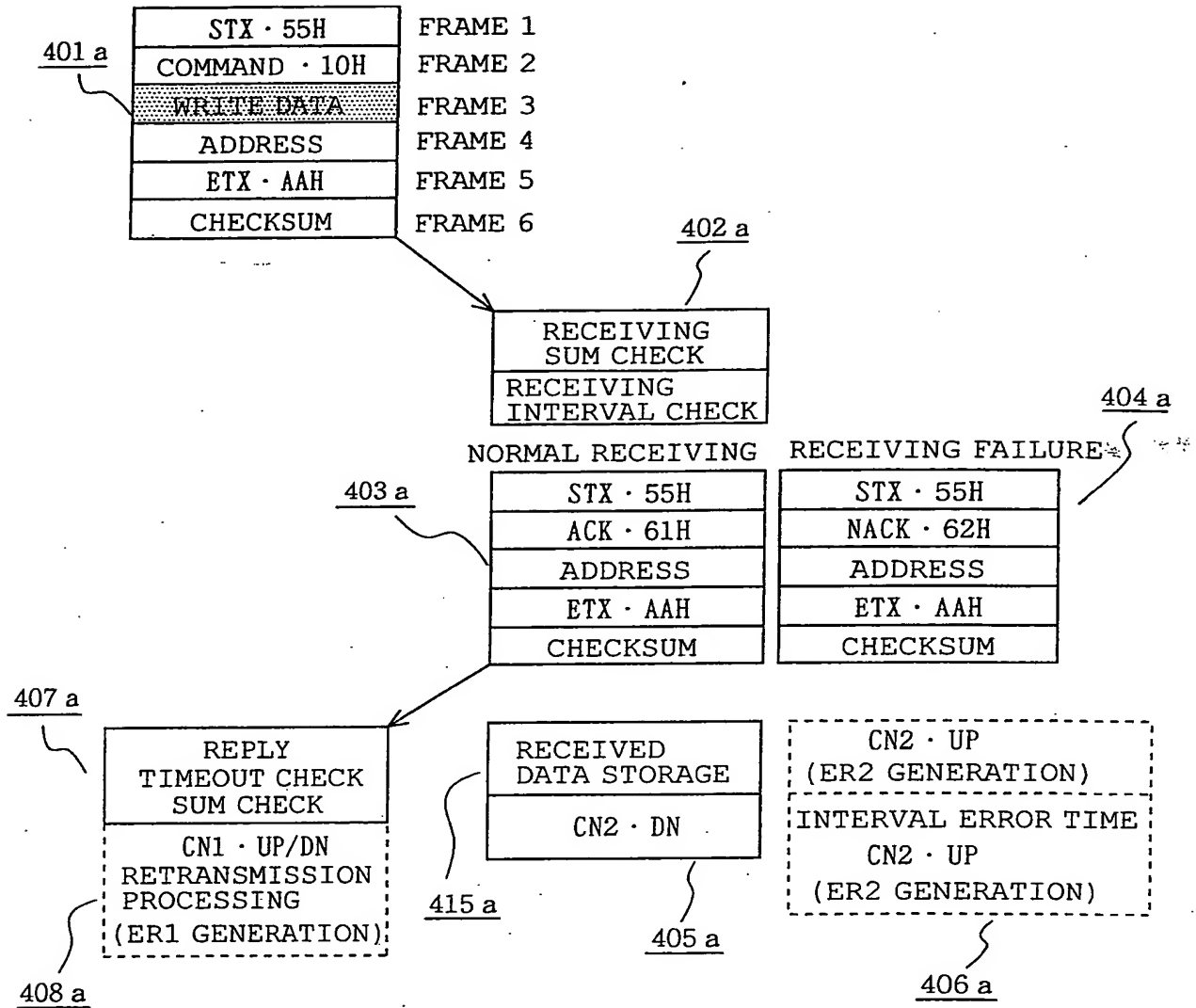


FIG. 4

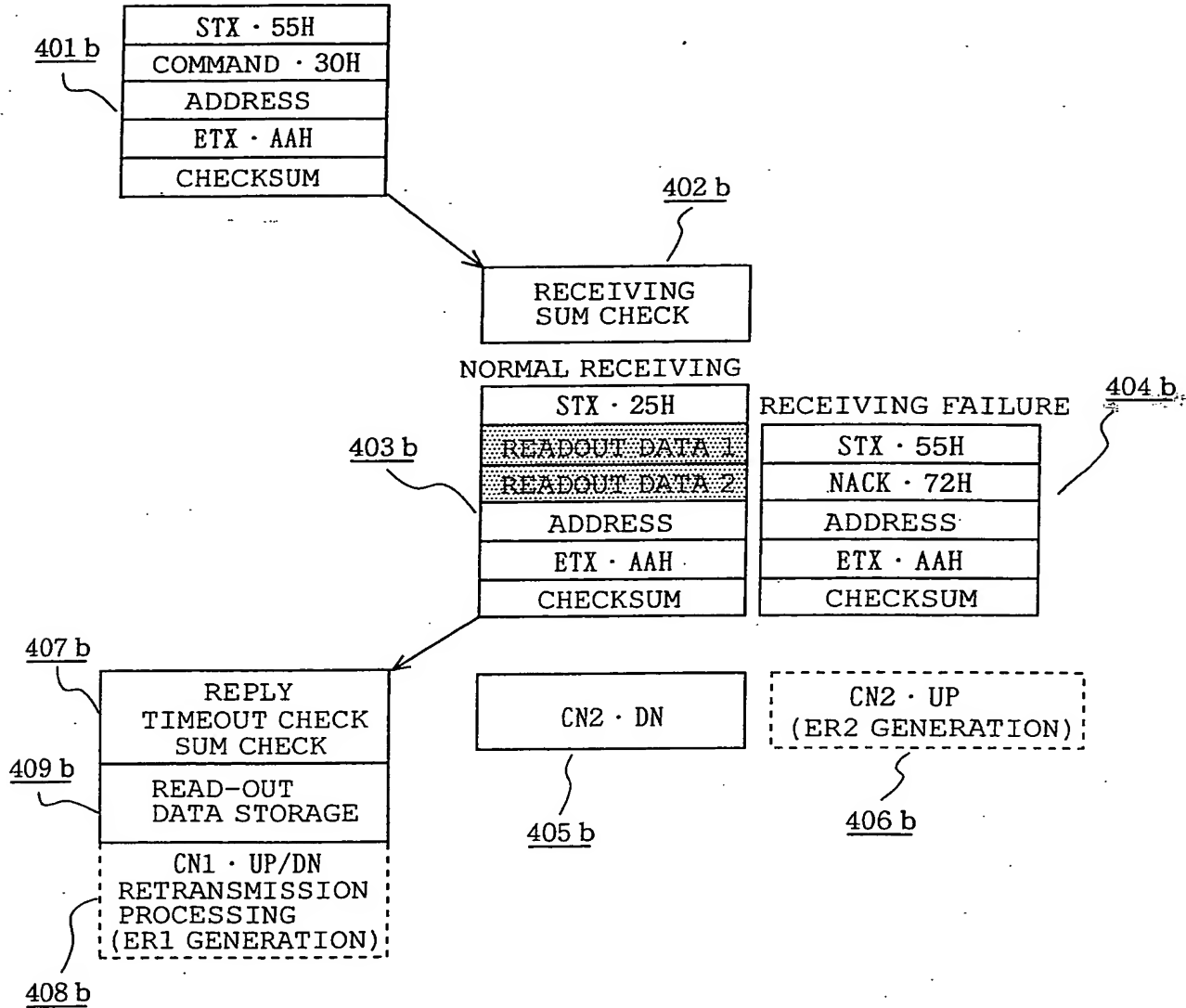


FIG. 5

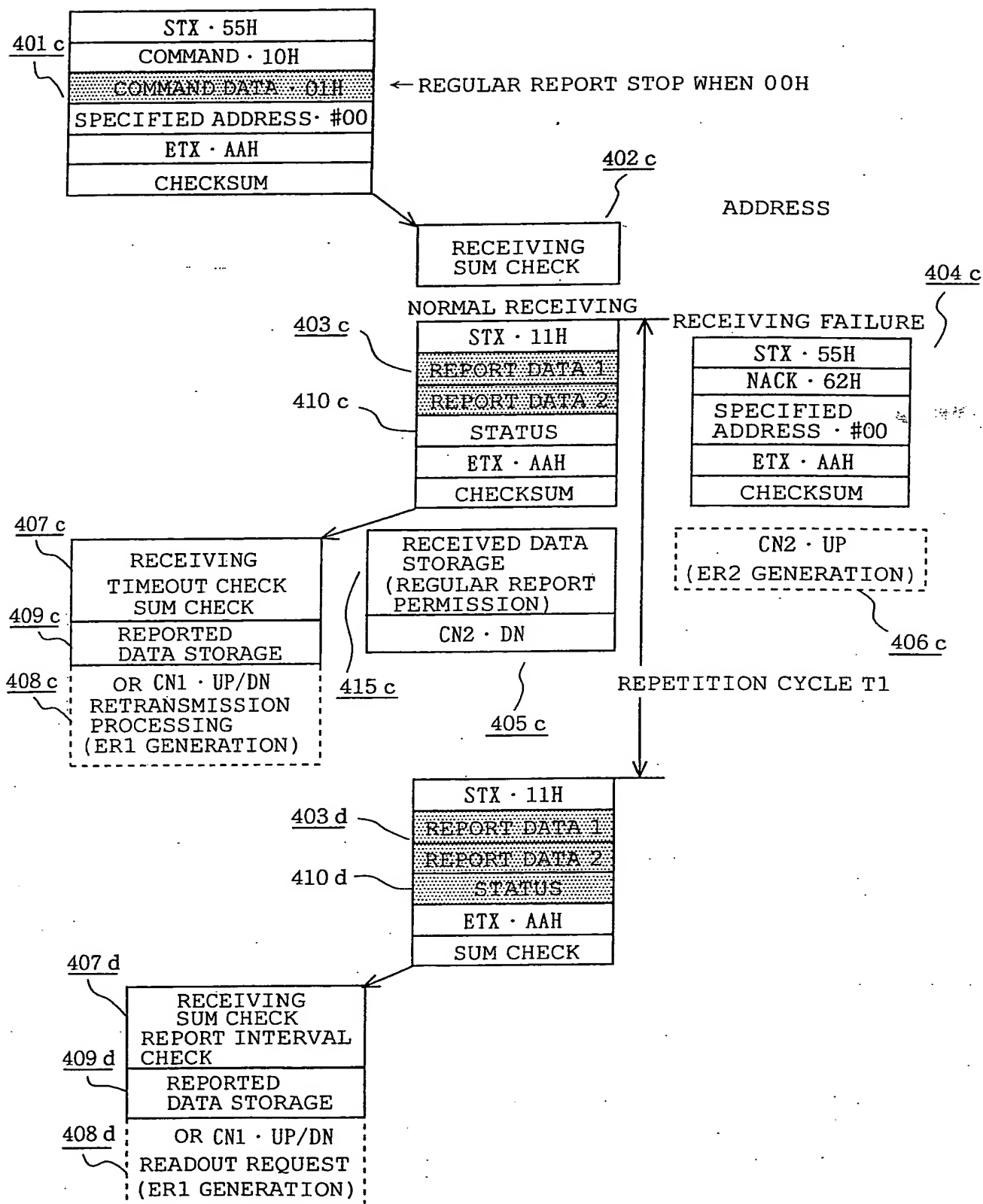


FIG. 6

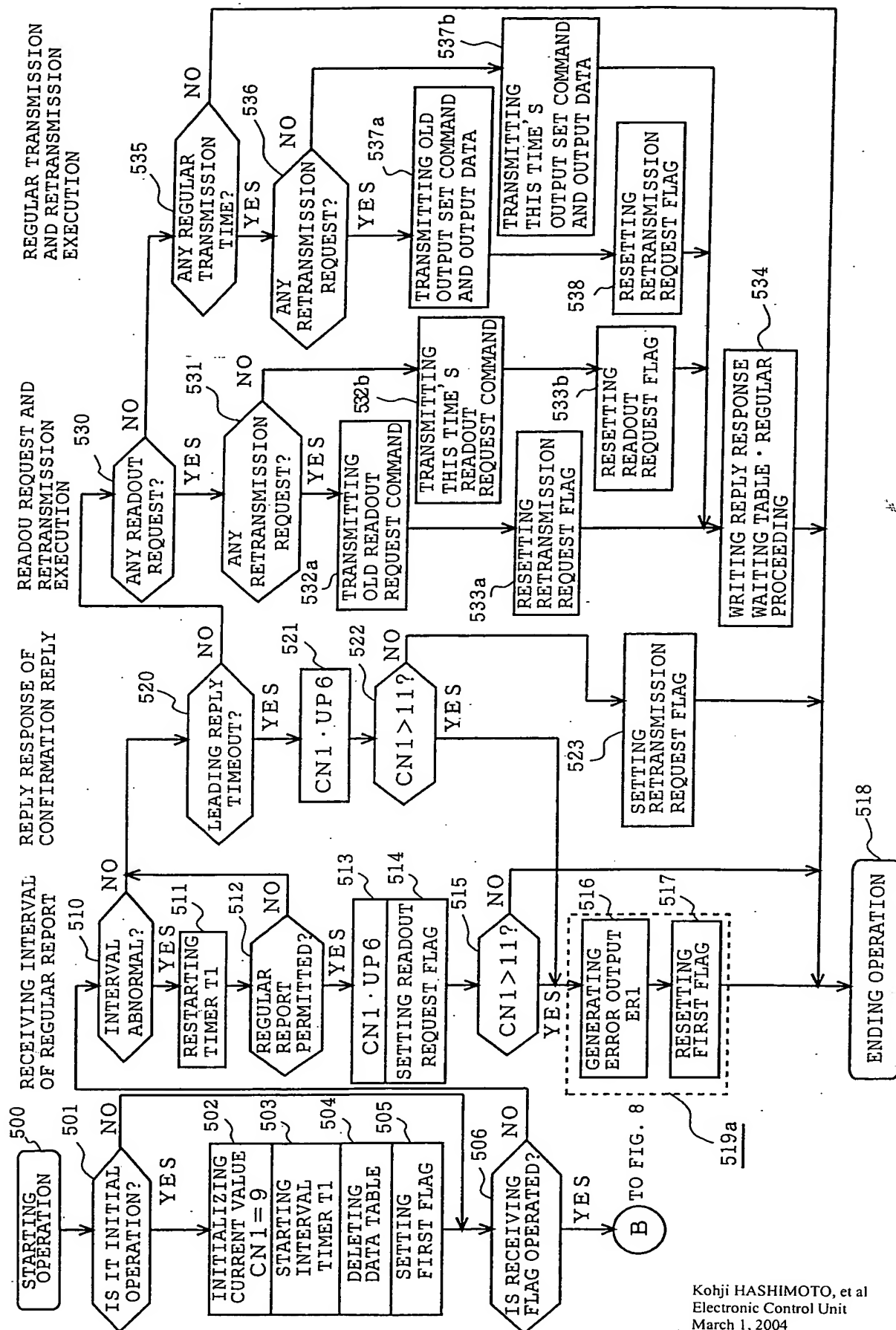


FIG. 7


$$\infty$$

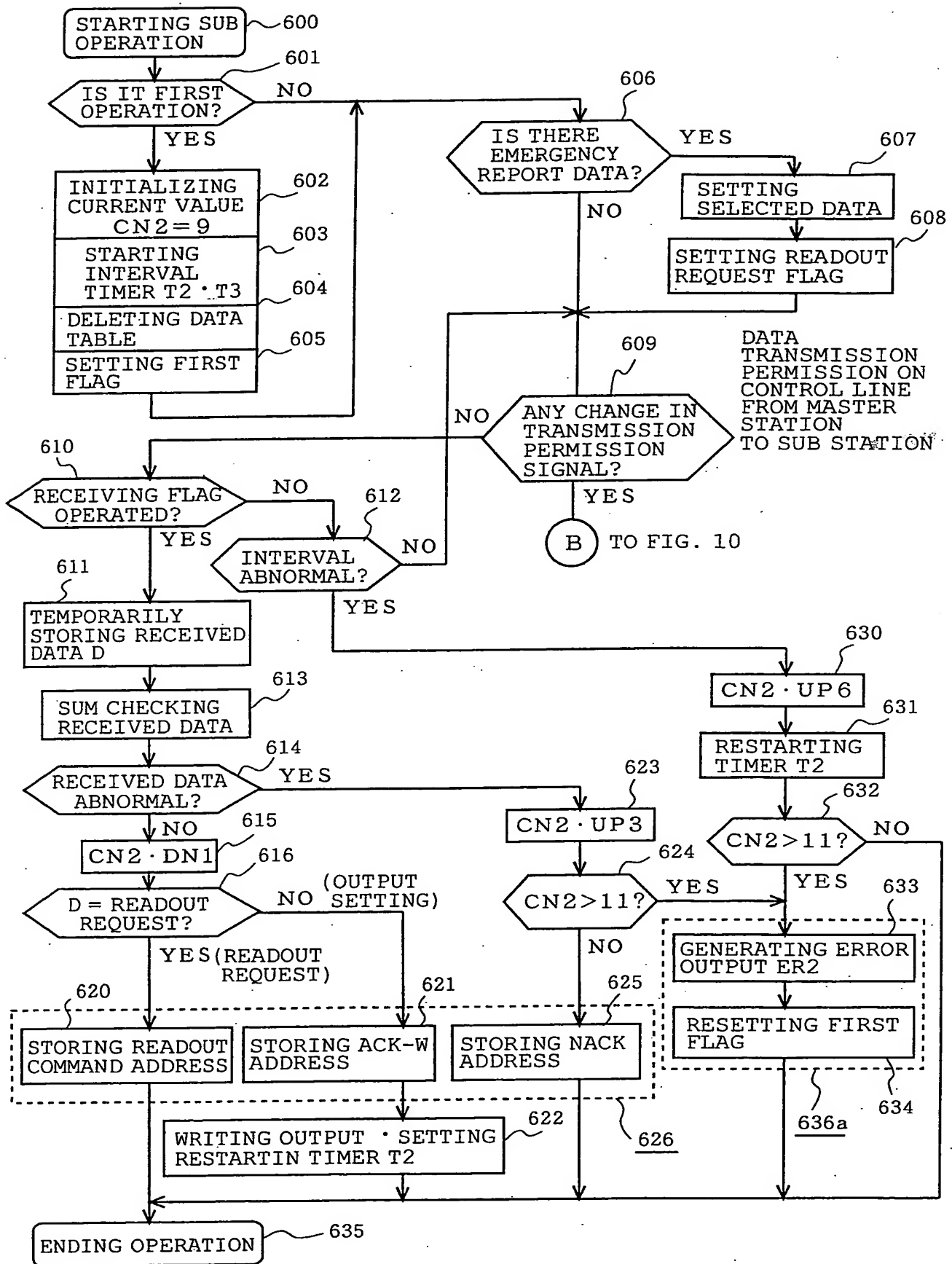


FIG. 9

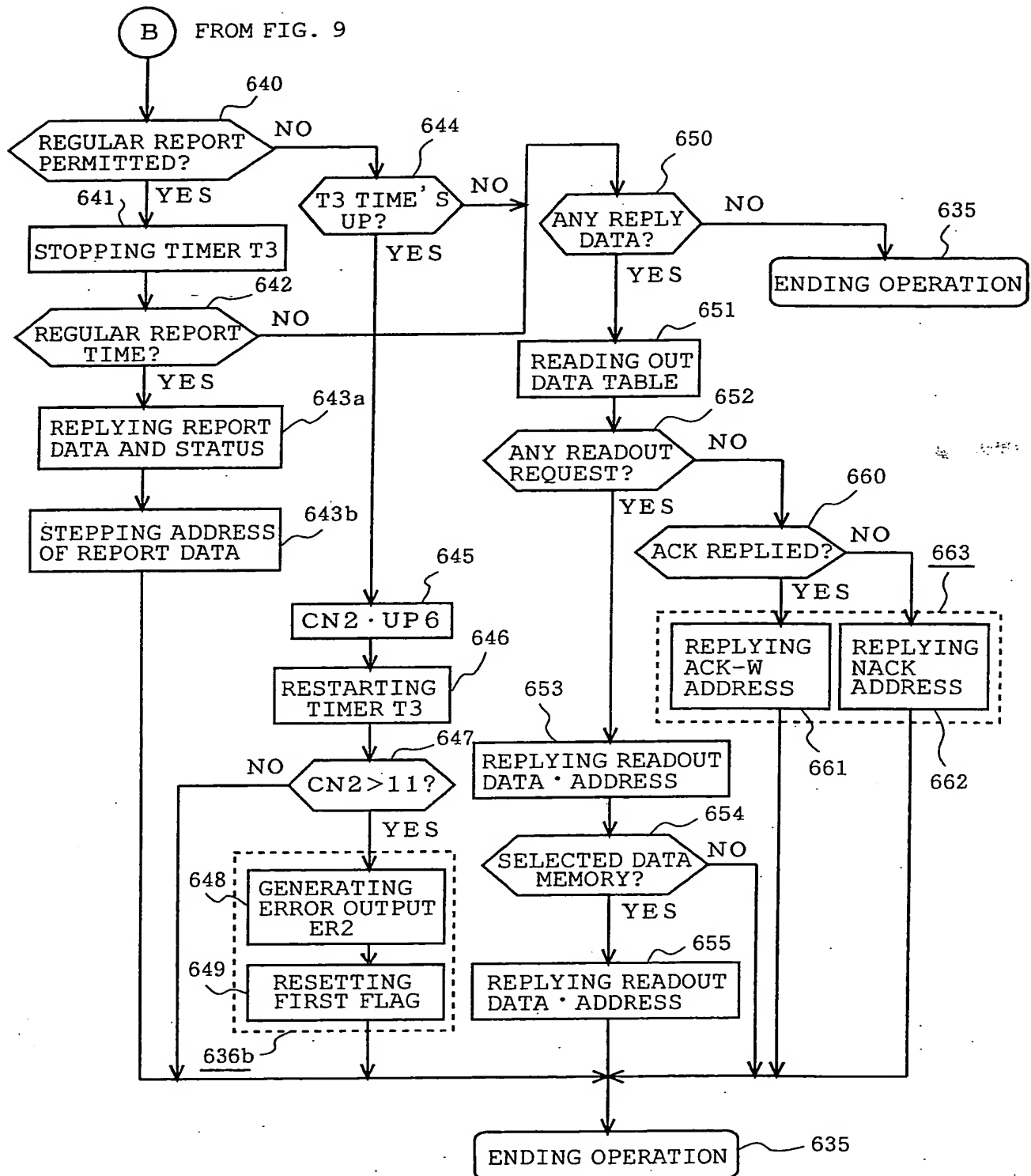


FIG. 10

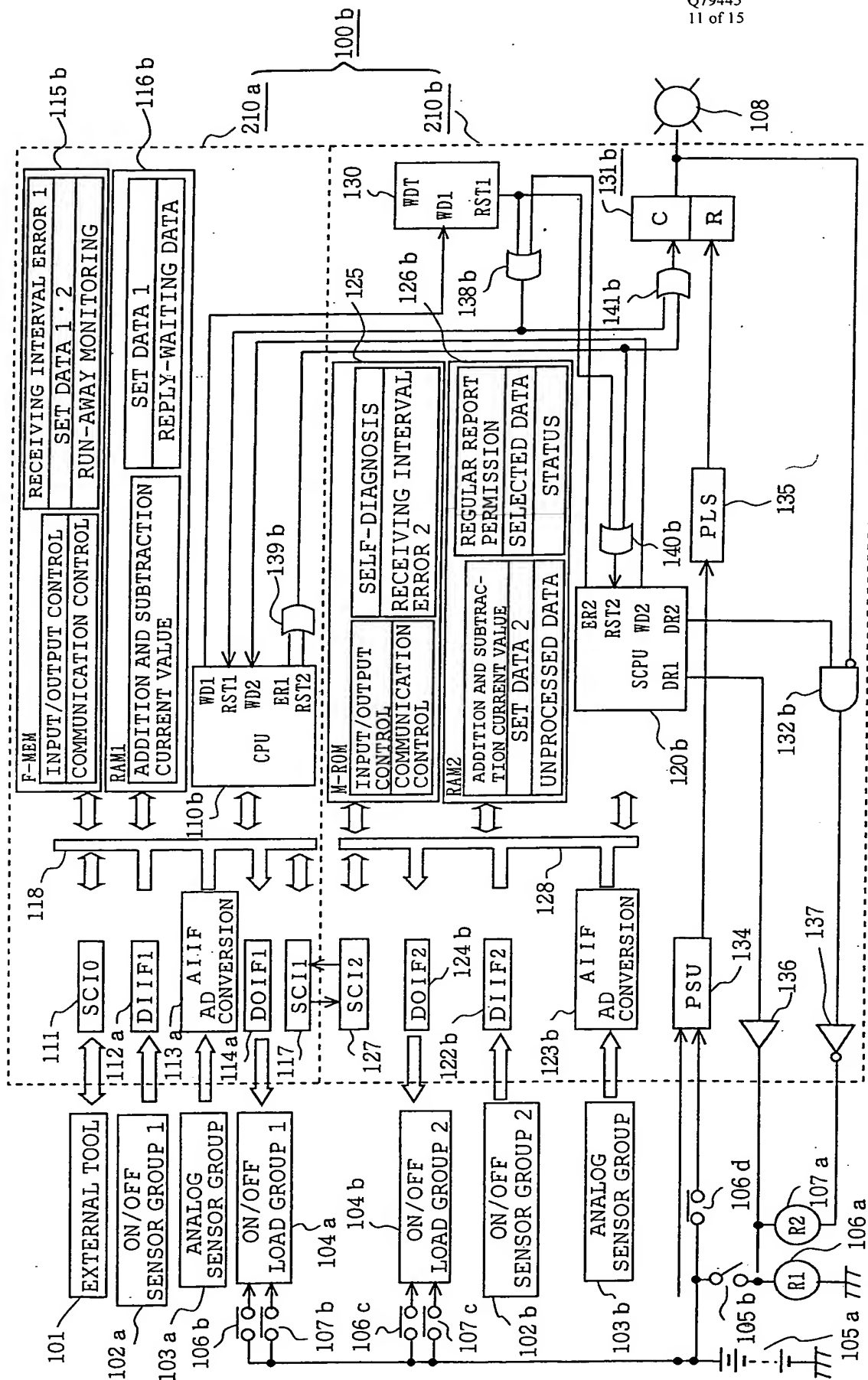


FIG. 11

ADDRESS	b7	b6	b5	b4	b3	b2	b1	b0	
00									REGULAR REPORT PERMISSION
01									NORMAL-SIDE LIMIT VALUE
02									ABNORMAL-SIDE LIMIT VALUE
03									INITIALIZATION VALUE
04									FIRST VARIATION VALUE
05									SECOND VARIATION VALUE
06									THIRD VARIATION VALUE
07									REPLY RESPONSE ACCEPTABLE TIME PERIOD
08									RECEIVING INTERVAL ACCEPTABLE TIME PERIOD
09									
0A	Y07	Y06	Y05	Y04	Y03	Y02	DR2	DR1	INDIRECT OUTPUT 1
0B	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10	INDIRECT OUTPUT 2

REGULAR TRANSMISSION ORDER IS ALTERNATE
 TRANSMISSION OF 0A AND 0B

FIG. 12

ADDRESS	b7	b6	b5	b4	b3	b2	b1	b0	
10	FLAG	INPUT ADDRESS				ADDITION AND SUBTRACTION CURRENT VALUE			STATUS MEMORY
		OH				OH			
11	X07	X06	X05	X04	X03	X02	X01	X00	INDIRECT OUTPUT 1
12	X17	X16	X15	X14	X13	X12	X11	X10	INDIRECT OUTPUT 2
	UPPER 8 BITS								ANALOG 1
	LOWER 8 BITS								
13	UPPER 8 BITS								ANALOG 2
	LOWER 8 BITS								
14	UPPER 8 BITS								ANALOG 3
	LOWER 8 BITS								
15	UPPER 8 BITS								ANALOG 4
	LOWER 8 BITS								
16	UPPER 8 BITS								ANALOG 5
	LOWER 8 BITS								
17	ADDRESS								SELECTED DATA MEMORY
	BIT SECTION				ERROR CODE				

FIG. 13

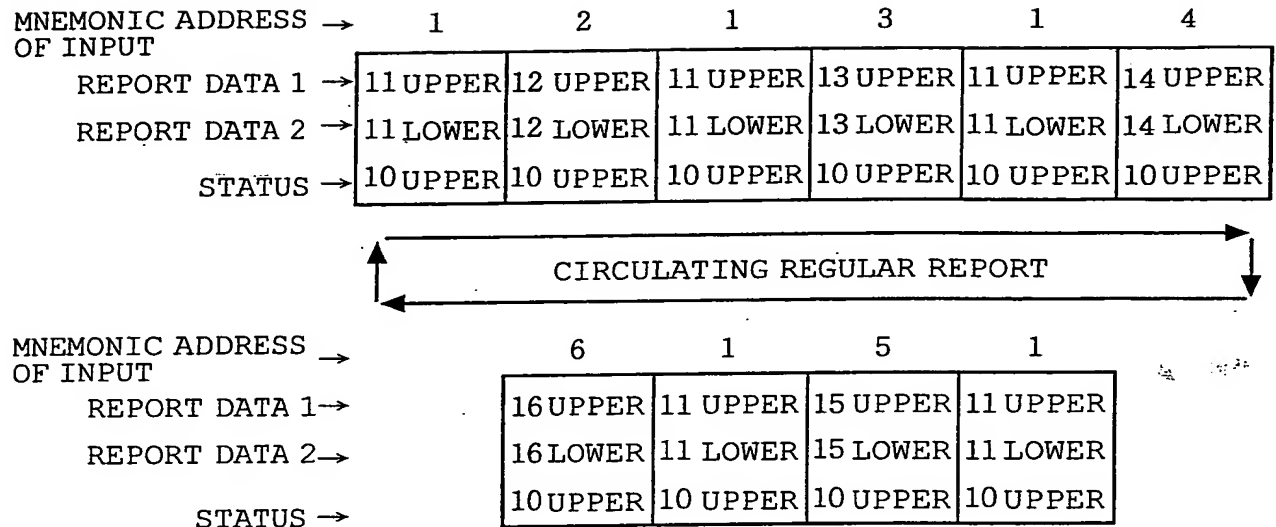


FIG. 14

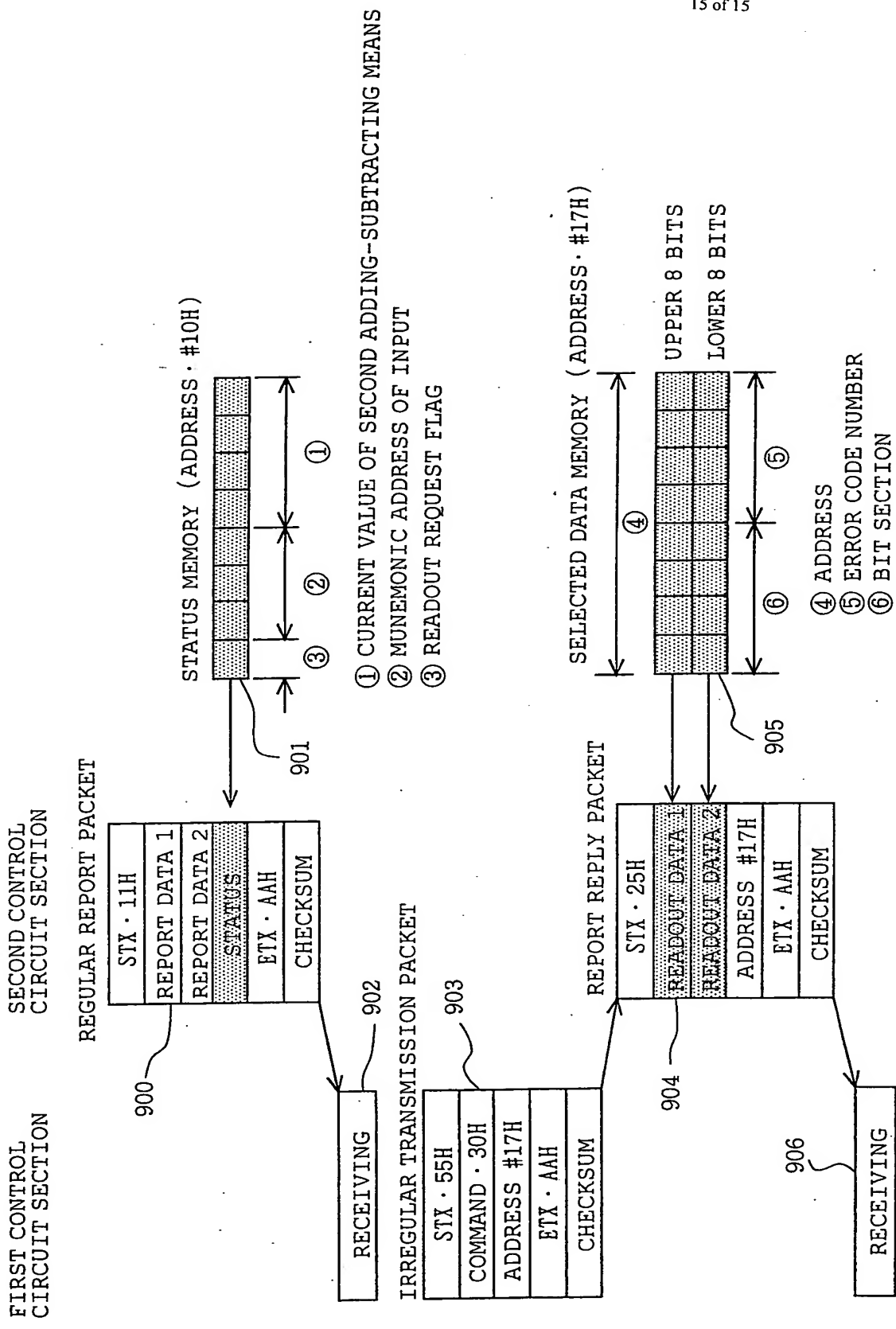


FIG. 15